ABSTRACT OF THE DISCLOSURE

A computer system has two CPUs. A shared memory exchanges data between the two CPUs. When the first CPU writes data in the shared memory, an address determination unit determines whether the address of the written data is in a predetermined area. A significance determination unit determines whether the written data is significant that should be immediately processed by the second CPU. If the address determination unit and the significance determination unit determine that the address is in the predetermined area and that the data is significant, an interrupt signal is supplied to an interrupt controller.